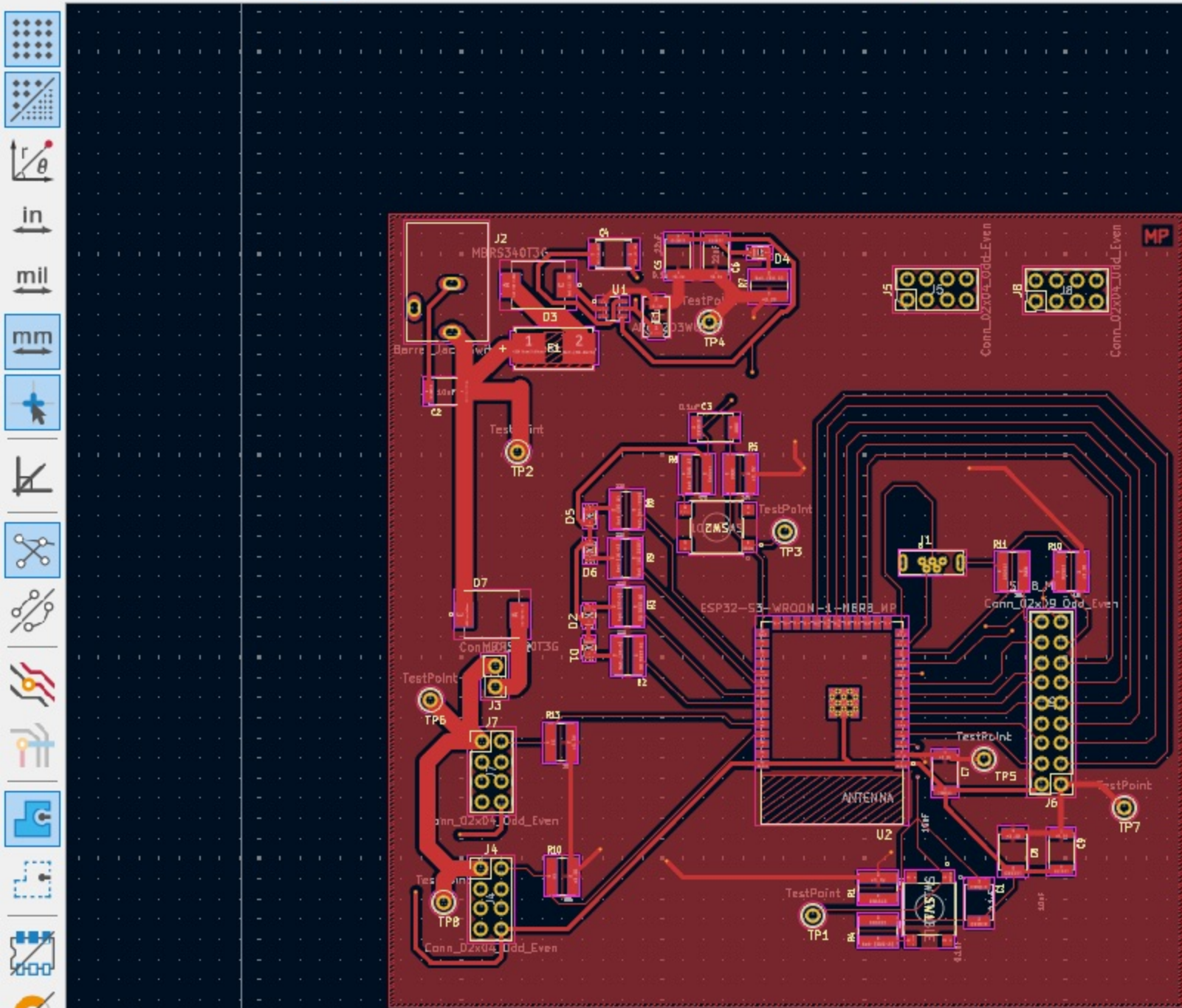




Track: use netclass width Via: use netclass sizes F.Silkscreen 0.0254 mm (0.0010 in) Zoom



| Pads | Vias | Track Segments | Nets | Unrouted |
|------|------|----------------|------|----------|
| 207 | 20 | 399 | 87 | 0 |

File 'C:\Users\Mihir\OneDrive\Documents\KiCad\Patel_EGR314\Patel_EGR314.kicad_p...

Z 1.50

X 73.8886 Y 19.3548

dx 73.8886 dy 19.3548 dist 76.3815

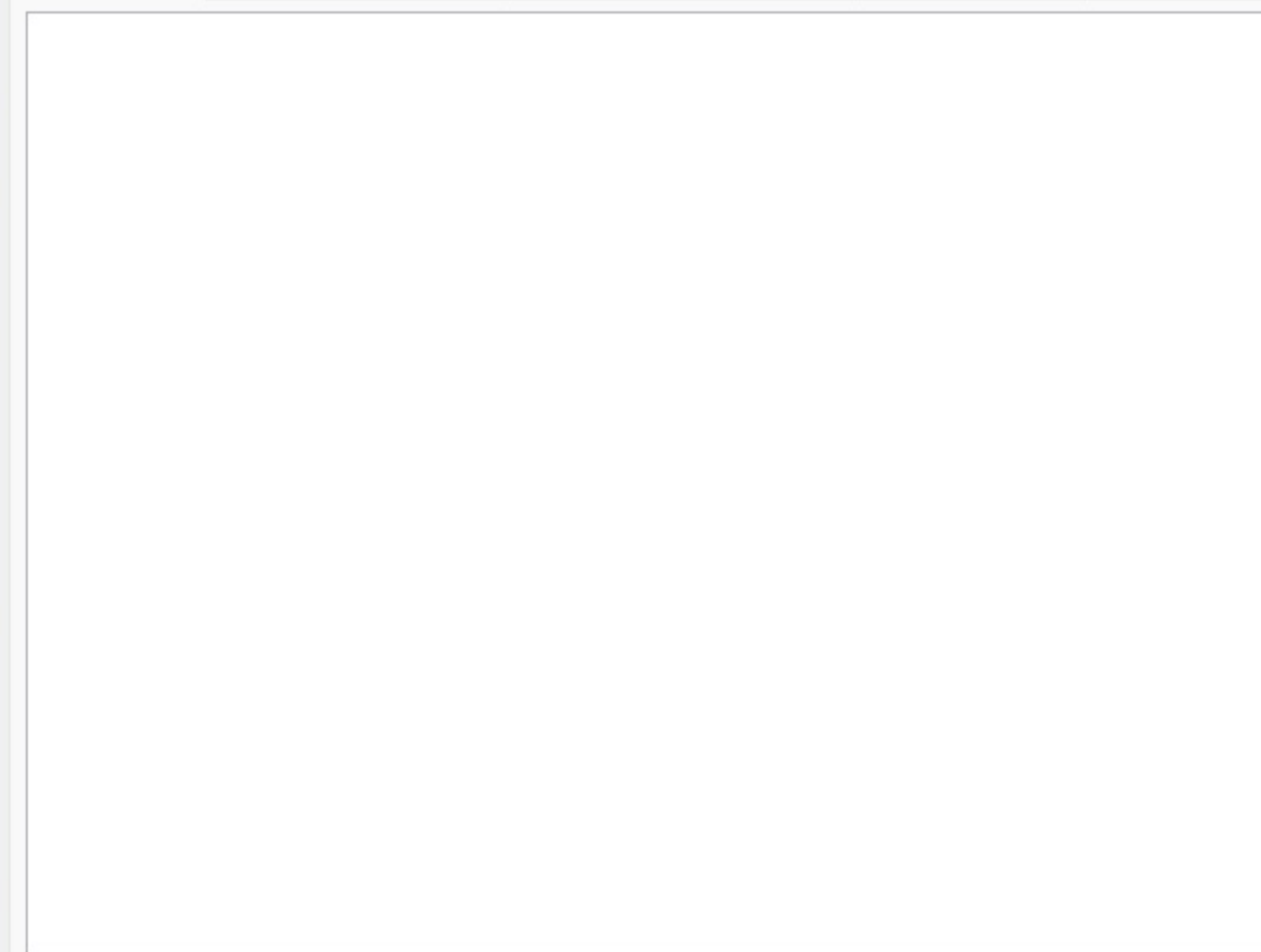
grid 0.0254

mm

Design Rules Checker

- ☒ Refill all zones before performing DRC ☐ Test for parity between PCB and schematic
- ☒ Report all errors for each track

Violations (0) Unconnected Items (0) Schematic Parity (not run) Ignored Tests (5)

Show: ☐ All ☒ Errors 0 ☒ Warnings 0 ☐ Exclusions

Save...

Delete Marker

Delete All Markers

Run DRC

Close

Appearance

Layers Objects Nets

- | | |
|-------------------------------------|---------------|
| <input checked="" type="checkbox"/> | F.Cu |
| <input checked="" type="checkbox"/> | B.Cu |
| <input checked="" type="checkbox"/> | F.Adhesive |
| <input checked="" type="checkbox"/> | B.Adhesive |
| <input checked="" type="checkbox"/> | F.Paste |
| <input checked="" type="checkbox"/> | B.Paste |
| <input checked="" type="checkbox"/> | F.Silkscreen |
| <input checked="" type="checkbox"/> | B.Silkscreen |
| <input checked="" type="checkbox"/> | F.Mask |
| <input checked="" type="checkbox"/> | B.Mask |
| <input checked="" type="checkbox"/> | User.Drawings |
| <input checked="" type="checkbox"/> | User.Comments |
| <input checked="" type="checkbox"/> | User.Eco1 |
| <input checked="" type="checkbox"/> | User.Eco2 |
| <input checked="" type="checkbox"/> | Edge.Cuts |
| <input checked="" type="checkbox"/> | Margin |
| <input checked="" type="checkbox"/> | F.Courtyard |
| <input checked="" type="checkbox"/> | B.Courtyard |

Layer Display Options

Inactive layers (H):

☒ Normal ☐ Dim ☐ Hide☐ Flip board view

Presets (Ctrl+Tab):

Front Layers

Viewports (Shift+Tab):

Selection Filter

- | | |
|--|---|
| <input checked="" type="checkbox"/> All items | <input type="checkbox"/> Locked items |
| <input checked="" type="checkbox"/> Footprints | <input checked="" type="checkbox"/> Text |
| <input checked="" type="checkbox"/> Tracks | <input checked="" type="checkbox"/> Vias |
| <input checked="" type="checkbox"/> Pads | <input checked="" type="checkbox"/> Graphics |
| <input checked="" type="checkbox"/> Zones | <input checked="" type="checkbox"/> Rule Areas |
| <input checked="" type="checkbox"/> Dimensions | <input checked="" type="checkbox"/> Other items |

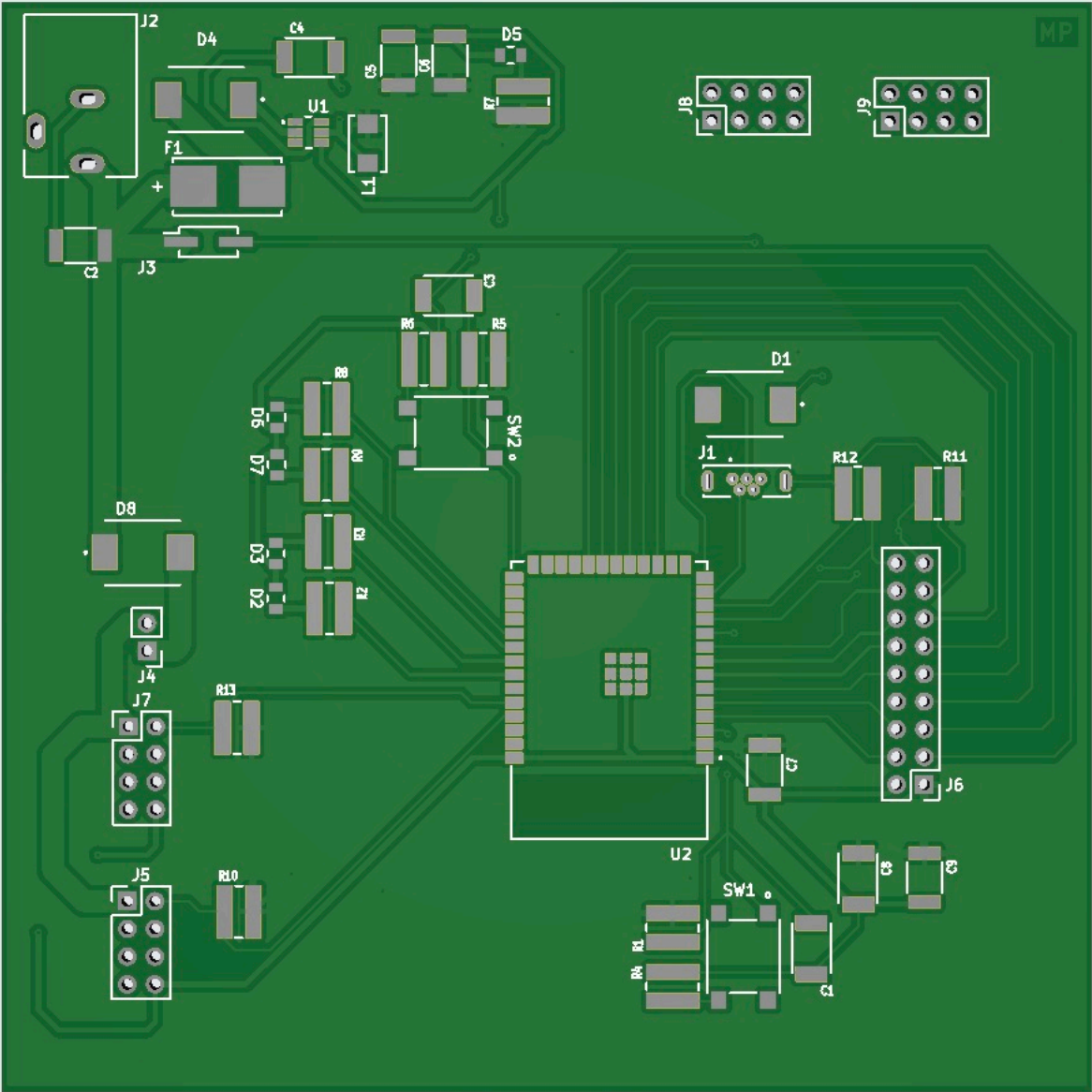
DFM check

Description | All

| Analyze project | Statistics | Operation |
|--|------------|-----------|
| Routing layer analysis | | |
| Sharp trace corner | 0, 3, 0 | Details |
| BGA pad | 0, 0, 0 | Details |
| Via placed within a pad | 0, 0, 0 | Details |
| Trace to board edge | 0, 0, 0 | Details |
| Trace spacing | 0, 0, 0 | Details |
| Unconnected trace end | 0, 3, 0 | Details |
| Trace width | 0, 0, 63 | Details |
| Fiducial | 0, 0, 0 | Details |
| Pad to board edge | 0, 0, 0 | Details |
| Pad spacing | 0, 0, 55 | Details |
| Plated through-hole to trace clearance | 0, 0, 0 | Details |
| Annular ring | 0, 24, 43 | Details |
| tht to smd | 0, 0, 21 | Details |
| Via to pad | 24, 0, 0 | Details |

Soldermask layer analysis

| | | |
|---|----------|---------|
| Soldermask bridge | 0, 0, 41 | Details |
| Solder mask opening exposing trace | 0, 0, 4 | Details |
| Soldermask opening with multiple segments | 0, 0, 0 | Details |
| Negative soldermask expansion | 0, 0, 0 | Details |



PCB DFM

SMT DFM

DFM check

Description All

| Analyze project | Statistics | Operation |
|-----------------|------------|-------------------------|
| tht to smd | 0, 0, 21 | Details |
| Via to pad | 24, 0, 0 | Details |

Soldermask layer analysis

| | | |
|---|----------|-------------------------|
| Soldermask bridge | 0, 0, 41 | Details |
| Solder mask opening exposing trace | 0, 0, 4 | Details |
| Soldermask opening with multiple segments | 0, 0, 0 | Details |
| Negative soldermask expansion | 0, 0, 0 | Details |

Silkscreen layer analysis

| | | |
|-----------------------|----------|-------------------------|
| Silkscreen to pad | 0, 50, 0 | Details |
| Silkscreen to hole | 0, 0, 0 | Details |
| Silkscreen line width | 0, 50, 0 | Details |

Drill layer analysis

| | | |
|-----------------------------|---------|-------------------------|
| Unconnected via | 0, 0, 0 | Details |
| Missing plated through-hole | 0, 0, 0 | Details |
| Unconnected via | 0, 0, 0 | Details |
| Plated through-hole spacing | 0, 0, 0 | Details |
| Short slot detection | 0, 3, 0 | Details |
| Slot width check | 2, 0, 3 | Details |
| Via to PTH spacing | 0, 0, 0 | Details |
| Unconnected via | 0, 0, 0 | Details |

Gerber

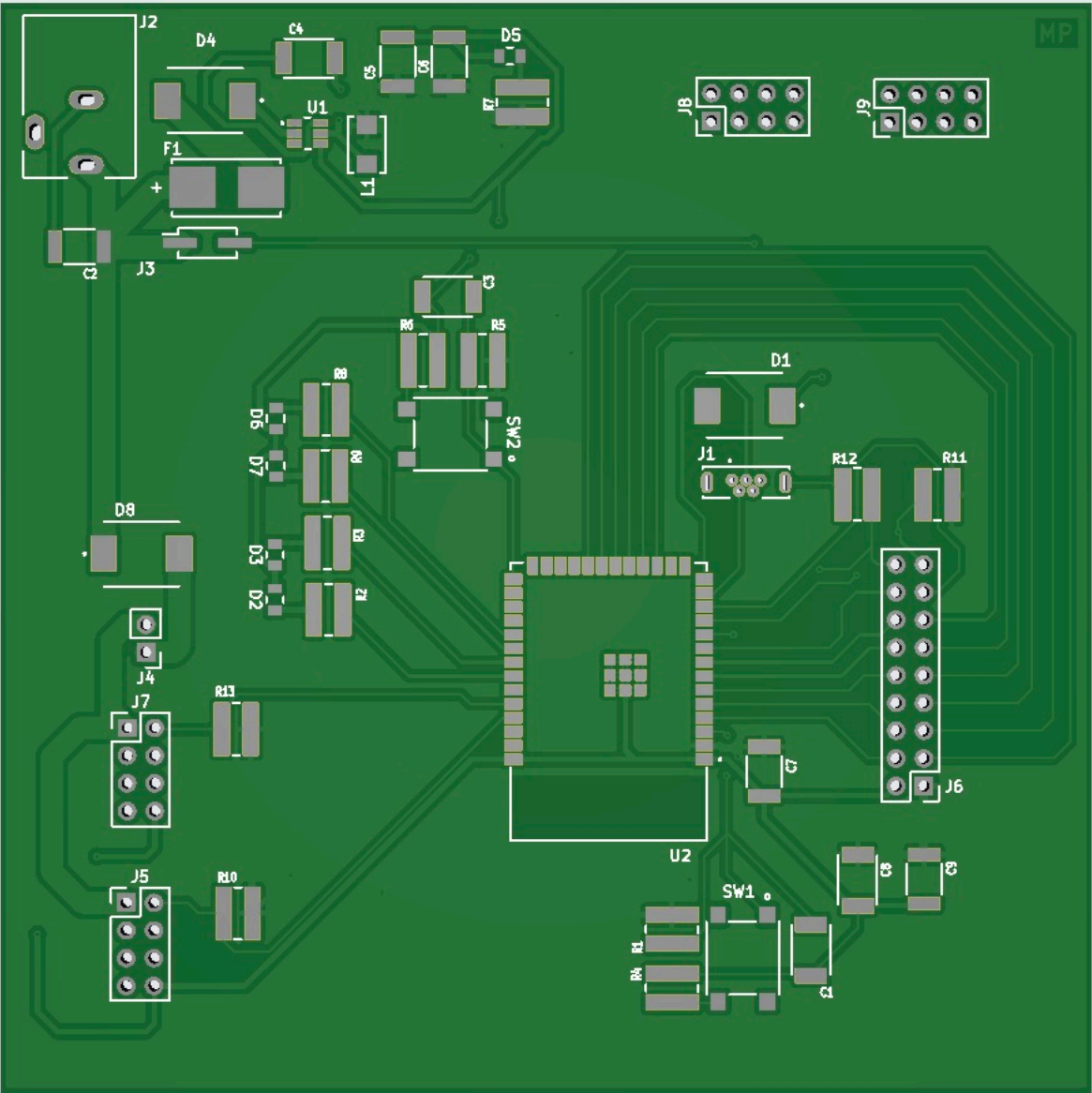
Wireframe

2D

3D

Top layer

Bottom layer





Schematic Hierarchy

Root (page 1)

Electrical Rules Checker

Violations (0) Ignored Tests (4)

Show: ☐ All ☒ Errors 0 ☒ Warnings 0 ☐ Exclusions

Save...

Delete Marker

Delete All Markers

Run ERC

Close

Selection Filter

- ☒ All items
- ☒ Symbols
- ☒ Wires
- ☒ Graphics
- ☒ Text
- ☒ Pins
- ☒ Labels
- ☒ Images
- ☒ Other items

